

# DESIGN NOTES

## Wide Input Range, High Efficiency DDR Termination Power Supply Achieves Fast Transient Response – Design Note 281

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### Introduction

Today's complicated computing and communication systems demand high system memory bandwidths. The emerging standard is Double Data Rate (DDR) memory because of its higher data rate and relatively low cost. A typical DDR memory system needs at least two main power supplies:  $V_{DD}$  for the I/O power and  $V_{TT}$  for the termination power. To ensure good signal quality and fast data rate, the termination power supply ( $V_{TT}$ ) must always track the  $V_{DD}$  with  $V_{TT} = V_{DD}/2$ .  $V_{TT}$  can be as low as 0.6V. Since the termination resistors can carry current in either direction, the  $V_{TT}$  power supply must be able to both source and sink current while tracking the  $V_{DD}$  supply. A family of new termination/tracking controllers, including the LTC<sup>®</sup>3717, LTC3718 and LTC3831, satisfy these DDR requirements.

### Overview of the LTC3717

The LTC3717 is a No  $R_{SENSE}$ <sup>™</sup> current mode synchronous buck tracking controller that senses inductor current via the  $R_{DS(ON)}$  of the bottom FET, eliminating the sense resistor and associated power loss. The LTC3717 implements a unique constant on-time architecture with

on-time programmed by the input voltage and output voltage. This scheme allows a fairly constant switching frequency while achieving an extremely fast load transient response. In addition, the controller's minimum on-time is less than 100ns, allowing for a very small duty cycle at a very high switching frequency, thus minimizing the size of the inductor and capacitors. This circuit is suitable for high step-down applications such as 20V input and 1.25V output.

The LTC3717 also includes a 5V internal LDO that can be used to drive an efficient logic-level power MOSFET. If an external 5V bias is available in the system, it can be applied to the  $EXTV_{CC}$  pin to disable the internal 5V LDO and reduce the power loss of the controller at high input voltage. The reference tracking input of the LTC3717 is attenuated 50% internally, achieving a 0.65% regulation accuracy and eliminating the need for an external 1:1 resistor divider in the DDR termination power supply design.

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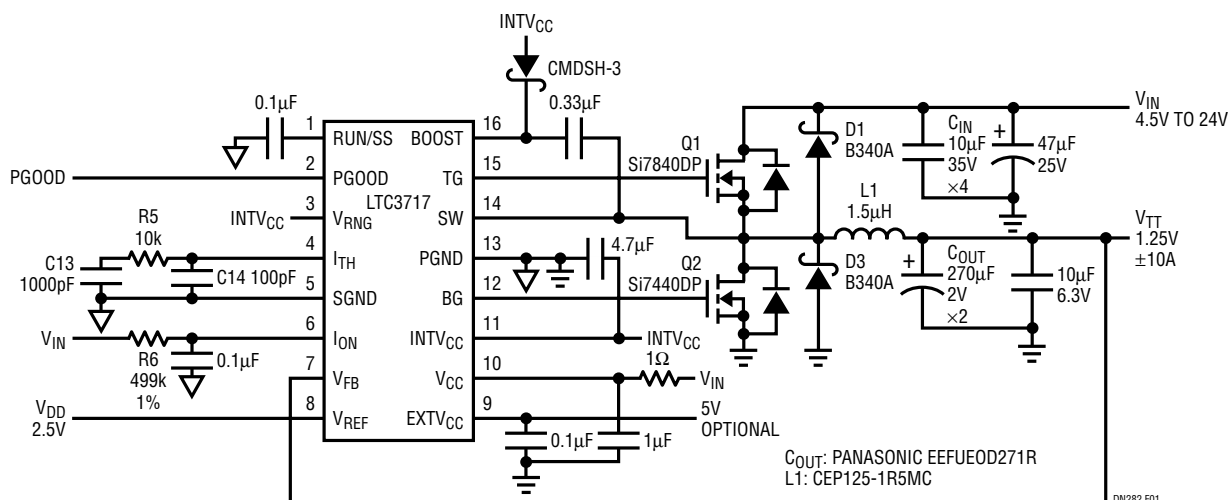


Figure 1. High Efficiency  $\pm 10A$  LTC3717  $V_{TT}$  Supply from 4.5V to 24V Input

## Design Example

Figure 1 shows a  $\pm 10A$  design using LTC3717. The input voltage can vary from 5V to 24V. The input voltage can be below 5V if an external 5V bias is available for powering the  $V_{CC}$  pin of LTC3717. This design uses only two SO-8 PowerPak MOSFETs from Siliconix to deliver  $\pm 10A$  current. To achieve a higher output current, use an inductor with a higher current rating and lower  $R_{DS(ON)}$  MOSFETs. This circuit achieves 84% efficiency at 250kHz switching frequency, 1.25V/10A output and 12V input, as shown in Figure 2.

The combination of the unique constant on-time current mode architecture of LTC3717 and the OPTI-LOOP<sup>®</sup> compensation design produces an excellent load transient

response. Figure 3 shows a typical load transient waveform. With only two SP output caps (270 $\mu F$ /2V), the output voltage variation is less than 100mV for a 10A load step.

## Conclusion

The LTC3717 DDR termination power supply achieves high efficiency and fast load transient response for high input applications. If the available power sources are less than 5V, the LTC3718 can be used. The LTC3718 integrates an LTC3717 controller with a 1.2MHz boost regulator for the 5V MOSFET gate power. If the input voltage is between 3.3V and 8V, the LTC3831, a voltage mode synchronous buck tracking controller, can also be used.

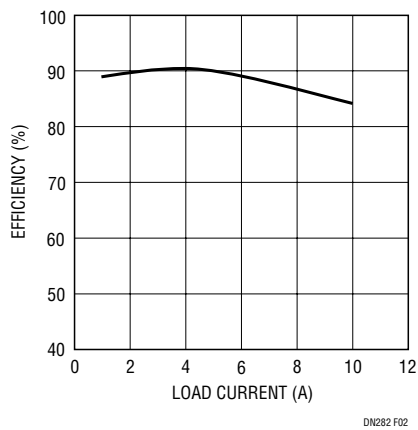


Figure 2. Measured Efficiency at 1.25V Output, 12V Input

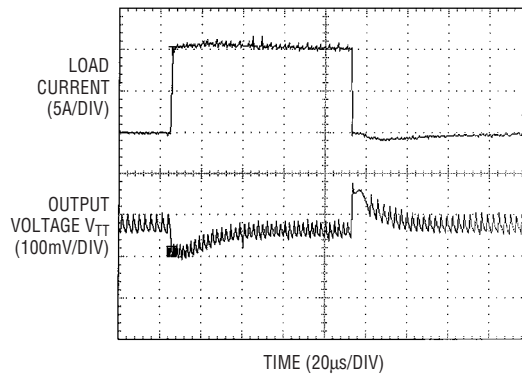


Figure 3. Load Transient Waveforms

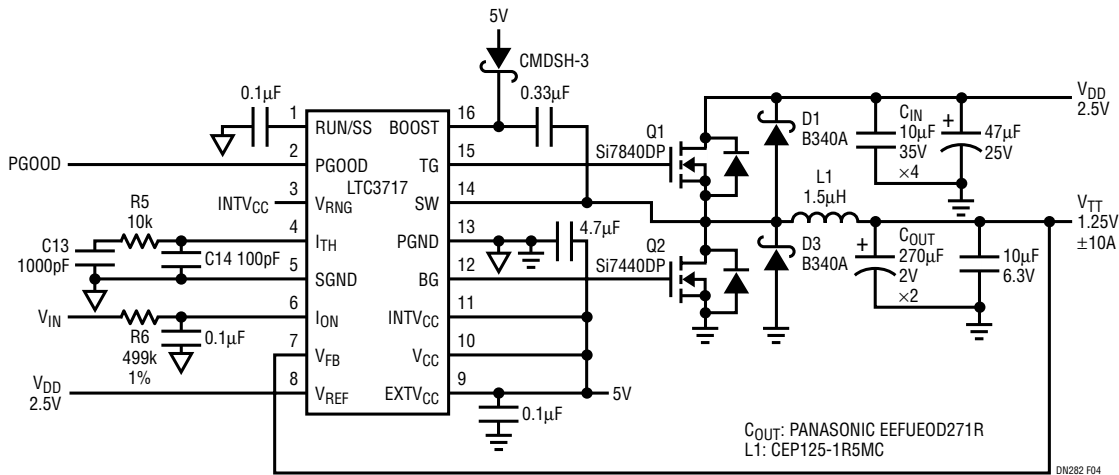


Figure 4. High Efficiency  $\pm 10A$  LTC3717  $V_{TT}$  Supply from  $V_{DD}$  Input

### Data Sheet Download

<http://www.linear.com/go/dnLTC3717>

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